REMARKS

Reconsideration of the application is respectfully requested.

The undersigned thanks Examiner Huisman for the courtesy of a telephone interview on or about the end of March 2004, in which claim 1 was discussed in view of the art reference U.S. Patent No. 6,374,349 issued to McFarling ("McFarling"). According to the Examiner, Applicant's claimed "updating" limitation in claim 1 (prior to entry of this amendment) reads on the "replacement" action in McFarling. The undersigned disagreed as this being an overly broad interpretation of the claim language "updating a field for a matching entry". The Examiner argued that the replacement in McFarling in essence "updates the cache" in that new prediction information is written for future use. That may be so, however the relevant claim language is *updating a field for a* ***matching entry*** . . . Note that a replacement creates a new entry, because there was no matching entry in the first place. Unfortunately, no agreement was reached between the undersigned and the Examiner. Applicant may file a continuation application to further pursue the cancelled claims 1-21.

In this amendment, Applicant has taken a different approach to overcoming the rejection in view of McFarling.

Referring now to new claim 22, a first prediction is obtained using a saturating counter branch predictor, and a second prediction using a local branch history table where the latter prediction is generated by a decision function based on a history value from a matching entry of the local branch history table. This decision function is implemented by combinational logic that has no memory so as to reduce on-chip area. The inventor has found through simulations that this combination of a saturating counter branch predictor and a *static* local branch history predictor permits a comparable prediction accuracy to be maintained but with less on-chip area than other hardware-based local history predictors. A significant reduction in on-chip area obtained by using the static predictor, that is one which implements a decision function by combinational logic that has no memory, allows the branch history table to be populated with a greater number of entries thereby improving the performance of the combination as a whole. McFarling does not teach or suggest such a combination.

It is noted that although the Examiner refers at page 13 of the Office Action to Fig. 10 of McFarling as allegedly teaching combinational logic coupled to an output of a history multiplexer to provide the second prediction (Fig. 10, prediction line 102 exiting from combinational logic that produces the taken/not-taken signal), Applicant respectfully disagrees that this teaches or suggests providing the second prediction as generated by a decision function that is implemented by combinational logic that has no memory, so as to reduce on-chip area. There is no teaching or suggestion to modify McFarling so that the prediction line 102 provides the recited capability of claim 22.

With respect to U.S. Patent No. 5,842,998 issued to Gochman, et al. ("Gochman"), which was relied upon by the Examiner in allegedly teaching as component 330 in Fig. 4A the claimed combinational logic, again Applicant respectfully disagrees because a review of Gochman did not reveal such specific capability.

Turning now to new claim 27, this claim is directed to a processor having saturating counter branch prediction logic and local branch history prediction logic. The local branch history prediction logic has a local branch history table to provide a taken/not taken history from a matching entry in the table in response to a hit. In addition, combinational logic is provided that is predetermined at the time the processor is built, to implement without memory a decision function whose output is the prediction of the local branch history predictor based on the taken/not taken history. Neither McFarling nor Gochman teach or suggest modifying a local branch history predictor in this manner and combining the local branch history predictor with a saturating counter branch predictor in the manner recited in new claim 27 where a prediction by either the saturating counter predictor or the local branch history predictor is selected, in response to a hit/miss indication, to be the prediction.

Turning now to new claim 35, this claim is directed at an apparatus having a local branch history predictor in which there is a means for generating without memory the prediction of the local branch history predictor based on a taken/not taken history from a local branch history table. Neither McFarling nor Gochman alone or in combination teach or suggest the combination recited in claim 35 that renders a prediction using means for providing a prediction based on the current state of a state machine and a local branch history predictor, where the latter is of the static variety

having means for generating without memory the prediction of the local branch history predictor.

Finally, turning now to new claim 40, a method is recited in which predictions are provided using a saturating counter branch predictor and a local branch history table. The prediction of the local branch history table is generated using a decision function based on a taken/not taken history value from a history field of a matching entry of the local branch history table. The decision function is implemented by combinational logic that has no counter or state machine. One of the two predictions is selected for the address, depending on whether or not the address resulted in a hit. Neither McFarling nor Gochman teach or suggest such a modification to the technique in McFarling of combining different predictor stages to yield a single prediction.

Any dependent claims not specifically mentioned above are submitted as not being anticipated or obvious in view of the relied upon art references for at least the reasons given in support of their base claims.

CONCLUSION

In sum, a good faith attempt has been made to present claims that are submitted to be in condition for allowance.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: April 21, 2004

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop Fee Amendment, Commissioner for Patents, Post Office Box 1450, Alexandria, Virginia 22313-1450, on April 21, 2004

Nadya Gordon 4/21/04

Nadya Gordon *April 21, 2004*